

AUGUST
2026



Collaborative Innovation in
3D VLSI Reliability (COIN-3D)

ISSUE #7



TBD



Sep 28 - Oct 2



2nd summer school on EDA Tool Customization for Complex Chiplet Architectures

Exploring the Future of Semiconductors



WELCOME TO OUR

Newsletter

We're glad you're
here again!



Dear readers,

Welcome to the 7th COIN-3D newsletter!

We are delighted to bring you another round-up of the latest achievements, activities, and insights from across our project. In this edition, you will find updates on our recent milestones, highlights from events, and a closer look at ongoing research shaping the future of 3D chiplet reliability. We appreciate your continued interest and invite you to stay connected with us through our social media channels for more news and discussions.

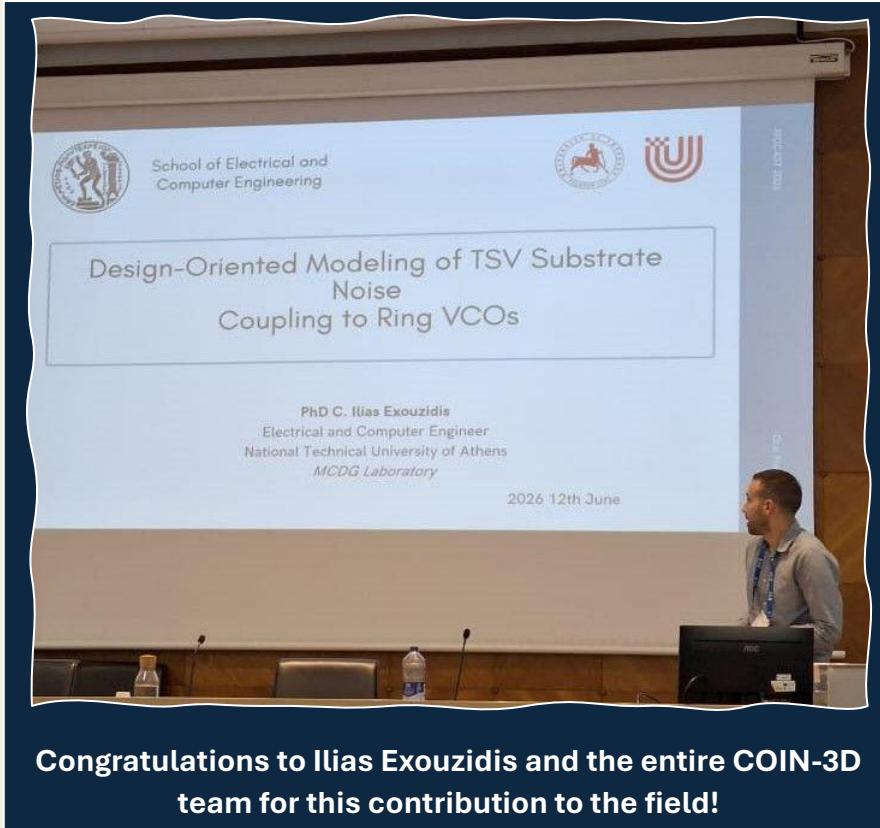
Yours sincerely,

The COIN-3D Team

In this newsletter you will find:

Events, conferences and more!

MOCAST 2026- Advancing 3D-IC Research



The **COIN-3D** project was proud to participate in the **15th International Conference on Modern Circuits and Systems Technologies (MOCAST 2026)**, held in Mallorca, Spain, from June 10–12, 2026.

At the conference, **PhDc researcher Ilias Exouzidis** presented the work “Design-Oriented Modeling of TSV Substrate Noise Coupling to Ring VCOs.”

This work addresses critical challenges in 3D-IC and Chiplet systems by proposing a closed-form three-port RLGC macromodel that explicitly exposes the substrate node.

Congratulations to Ilias Exouzidis and the entire COIN-3D team for this contribution to the field!

SMACD 2026-Power Delivery Network Optimization



The **COIN-3D** project was proud to participate in **SMACD 2026 (Smart Modeling and Applications in Circuit Design)**, held in Dresden, Germany.

At the conference, **PhDc researcher Maria Pantazi Kupraiou** presented the work “Workload-Aware Early-Stage Power Delivery Network Optimization via Architectural Power Traces.”

This work introduces a novel early-stage methodology that leverages architectural power traces to guide Power Delivery Network (PDN) design decisions before detailed physical implementation. The proposed approach represents an important step toward reliability-aware EDA methodologies for 2.5D and 3D integrated systems.

Congratulations to Maria Pantazi Kupraiou for this valuable contribution to the field!

ACACES 2026

The HiPEAC Summer School

Maria Pantazi from the COIN-3D project had the honor of representing our research group at **ACACES 2026, the prestigious HiPEAC Summer School**. ACACES brings together early-career researchers, students, and leading experts in computer architecture and systems from around the world, creating an invaluable platform for knowledge exchange and collaboration.

Maria presented her work, named **"HotPROTON: A System-Level Framework for Thermal-Aware Electromigration Analysis in Manycore Systems."** This work addresses the critical challenge of electromigration in large-scale manycore processors by integrating thermal effects into the analysis framework. HotPROTON provides system-level insights that help designers understand and mitigate electromigration risks—a growing concern as chip density and power consumption continue to increase.

The collage consists of three main images. On the left is a white tote bag with a blue strap and a blue lanyard. A badge hangs from the strap, reading "ACACES2026 Maria Pantazi-Kypariou University of Thessaly Greece July 12/18, 2026 - 18/20 July". The bag features the HiPEAC logo and the website "hipeac.net". In the center is a photograph of Maria Pantazi, a woman with dark hair and glasses, wearing a white sleeveless top and dark trousers, smiling. She is wearing the same blue lanyard and badge. On the right is a large presentation poster titled "A System-Level Framework for Thermal-Aware Electromigration Analysis in Manycore Systems". The poster lists authors: Maria Pantazi, Olympia Axelou, George Flores, Yuan Shen, Simon Polstra, George Stournioulis, and Anuj Pathania. It includes affiliations: University of Thessaly, Greece; Trinity College Dublin, Ireland; and University of Amsterdam, The Netherlands. The poster is divided into sections: 1. Motivation, 2. Key Contributions - HotPROTON, 3. HotPROTON Framework Overview, 4. PGN Generator - From Architecture to SPICE, 5. Physics-based EM Modeling, 6. Powergrid Mapping, 7. TTF & R-value Evaluation, 8. Experimental Results, and REFERENCES. It contains various diagrams, charts, and equations, including the MTTF equation: $MTTF = \frac{1}{\lambda} e^{\frac{a}{bT}} e^{\frac{c}{d(T-T_0)}} e^{\frac{e}{f(T-T_0)^2}}$. A blue box in the bottom right corner contains the text: "More Info: <https://www.hipeac.net/acaces/2026> /#/"

TWINRELECT PhD Forum



Two researchers from the **COIN-3D project** participated in the **PhD Forum at the 2nd TWINRELECT Scientific Workshop**, showcasing innovative research at the intersection of reliability, machine learning, and VLSI design. The workshop brought together leading researchers and PhD students to discuss the latest advances in electronic systems and AI-driven design methodologies.

Foteini Oikonomou from the **University of Thessaly** presented "**Adaptive Region-Aware Reinforcement Learning for Multi-Objective VLSI Placement Refinement.**" This work explores how reinforcement learning can be applied to optimize chip placement decisions, balancing multiple design objectives such as power, performance, and area. The presentation highlighted the potential of AI-driven techniques to enhance traditional EDA methodologies.

Nikolaos Kostakis also presented on "**Hardware Design & Acceleration in the AI era**" addressing how modern hardware design must evolve to support emerging AI workloads. His presentation examined the challenges and opportunities in designing efficient hardware accelerators and systems optimized for AI applications.

1st Scientific Webinar

COIN-3D

Collaborative Innovation in 3D VLSI Reliability

WEBINAR

Modern Physical Design: Bridging Design Flows and 3D Integration



28

August 2026
12:00 - 13:15 CET



George Goudroumanis
PhD Researcher

"Physical Design Multilevel Flow: From Synthesized Verilog to GDSII"



Maria Pantazi
PhD Researcher

"Enabling 3D Heterogeneous Placement in OpenROAD Using a 2D Placement Flow"



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On 28 August 2026, COIN-3D hosted its **1st Scientific Webinar**, bringing together researchers and practitioners to discuss advances in modern physical design and their extension towards 3D integration.

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The webinar featured two technical talks by researchers from the University of Thessaly.

1. **George Goudroumanis** presented a multilevel physical design flow, covering the complete journey from synthesized Verilog to GDSII.
2. **Maria Pantazi** shared her work on enabling 3D heterogeneous placement in OpenROAD by leveraging an existing 2D placement flow.

Upcoming Events

2nd COIN-3D Summer School



Our **2nd COIN-3D Summer School** will take place from **September 28 to October 2**. This intensive week-long program will bring together students and researchers to explore cutting-edge **EDA tool customization techniques for complex chiplet architectures**.

DSD & ICECS 2026

COIN-3D will be present at **DSD 2026**, the *29th Euromicro Conference Series on Digital System Design*.



2-4 September
Krakow, Poland

COIN-3D will also be present at **ICECS 2026**, the *29th Euromicro 33rd IEEE International Conference Series on Digital System Design Electronics Circuits and Systems*.



8-11 November
Thessaloniki, Greece



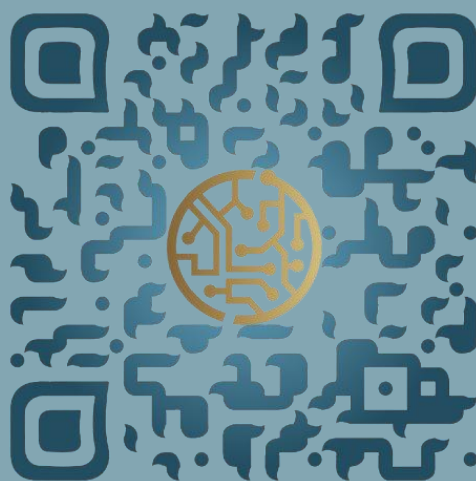
At ICECS 2026, COIN-3D will deliver a hands-on tutorial entitled:

“Open-Source Physical Design Flows for Monolithic and Heterogeneous 3D ICs using OpenROAD.”

The tutorial will showcase practical methodologies and workflows using OpenROAD to enable efficient physical design for both monolithic and heterogeneous 3D ICs.

COIN-3D

Exploring the future of semiconductors



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